

FIG. 1

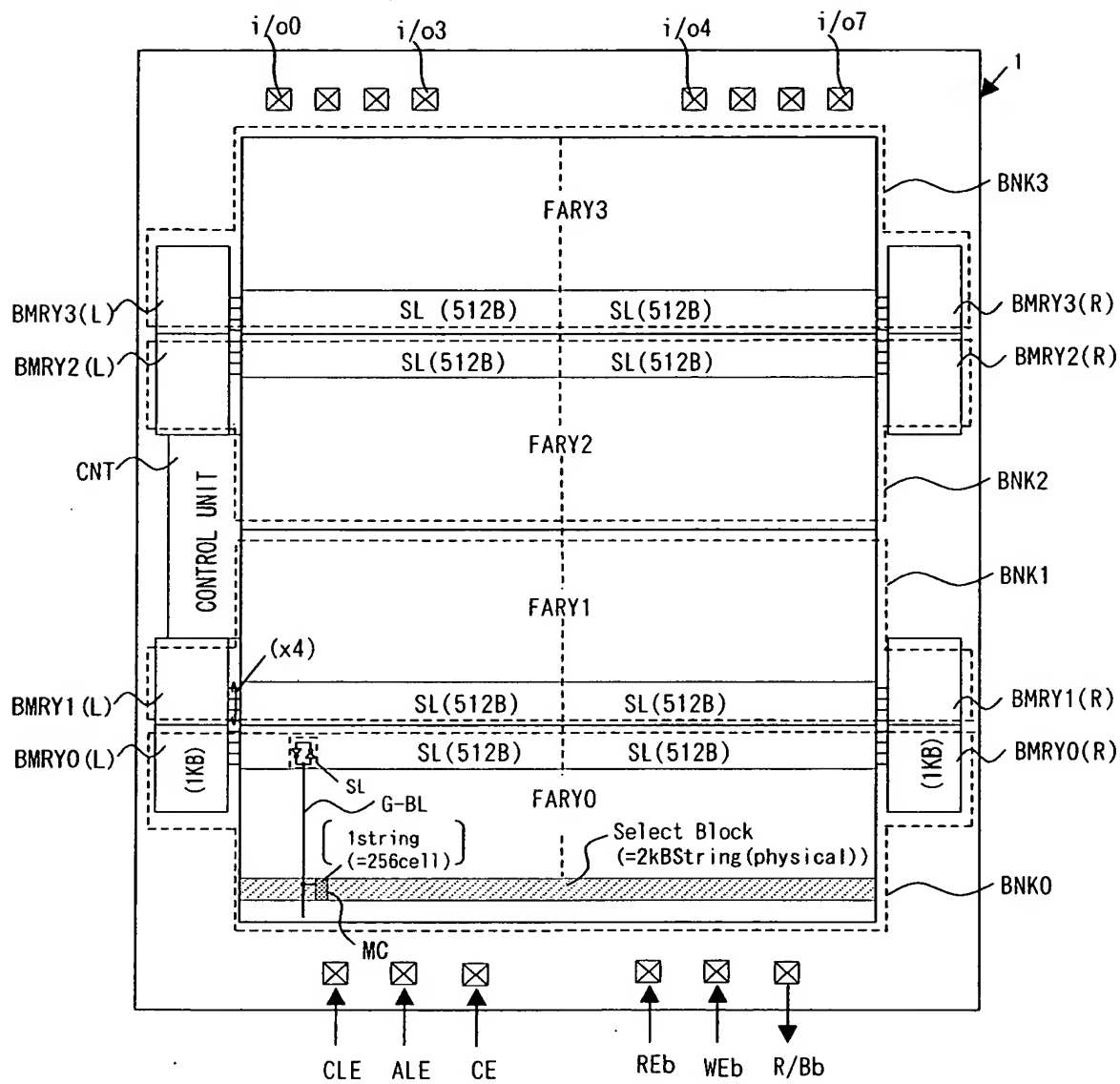


FIG. 2

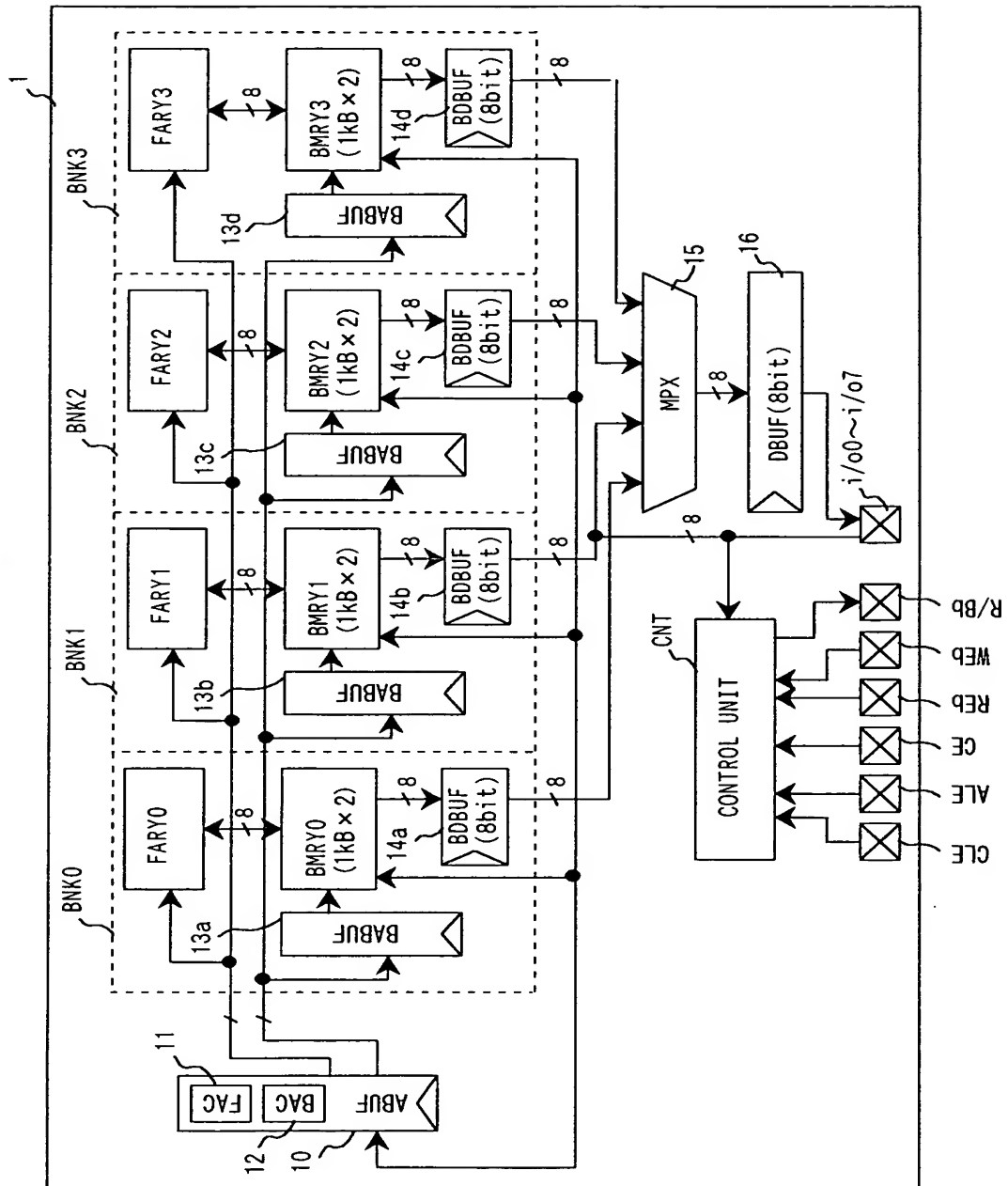


FIG. 3

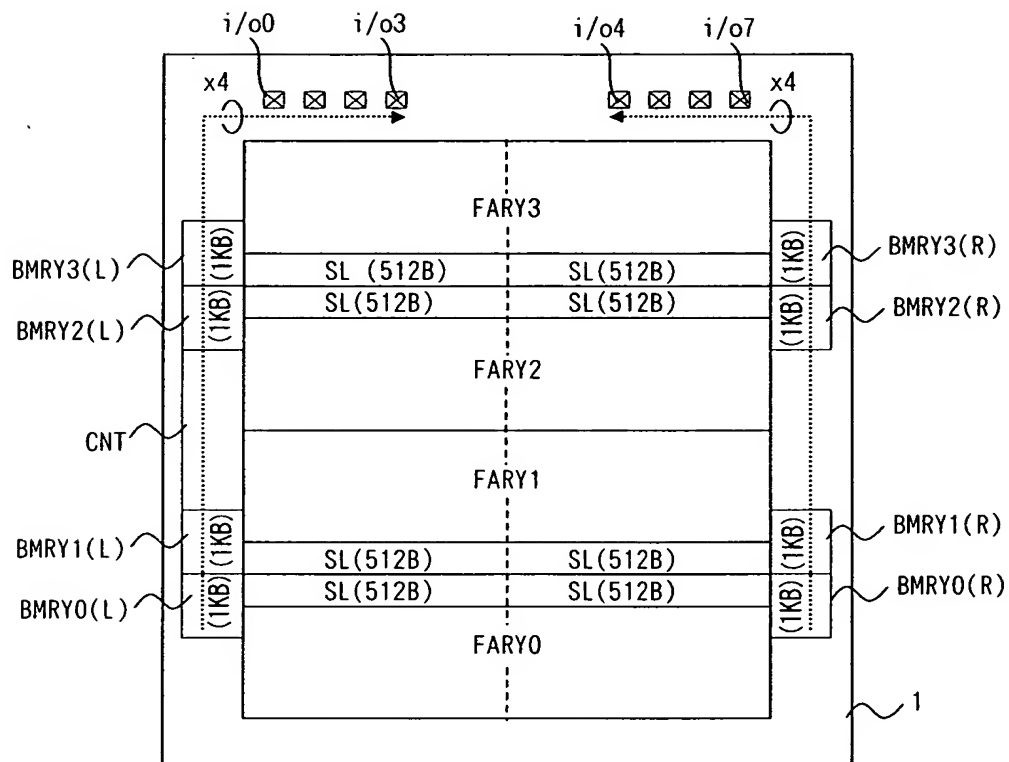


FIG. 4

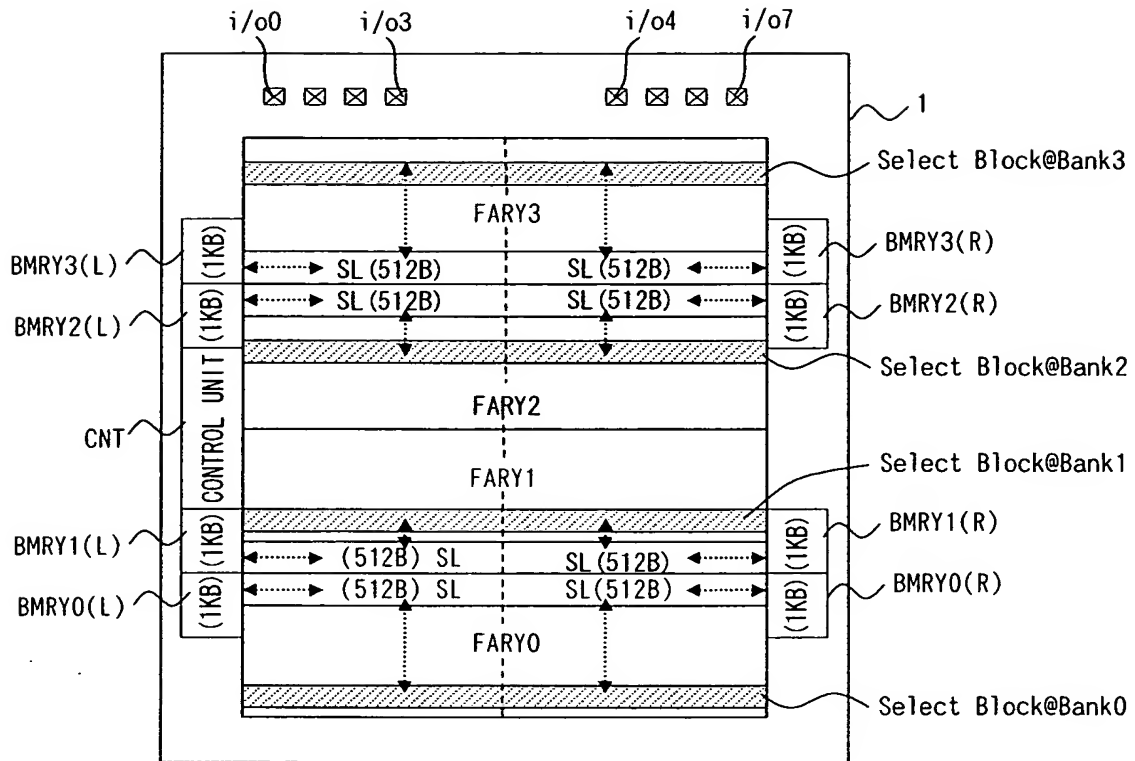


FIG. 5

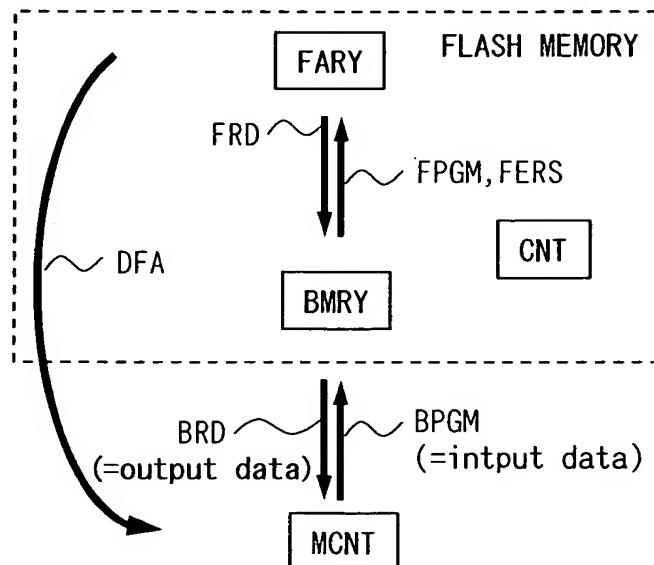


FIG.6

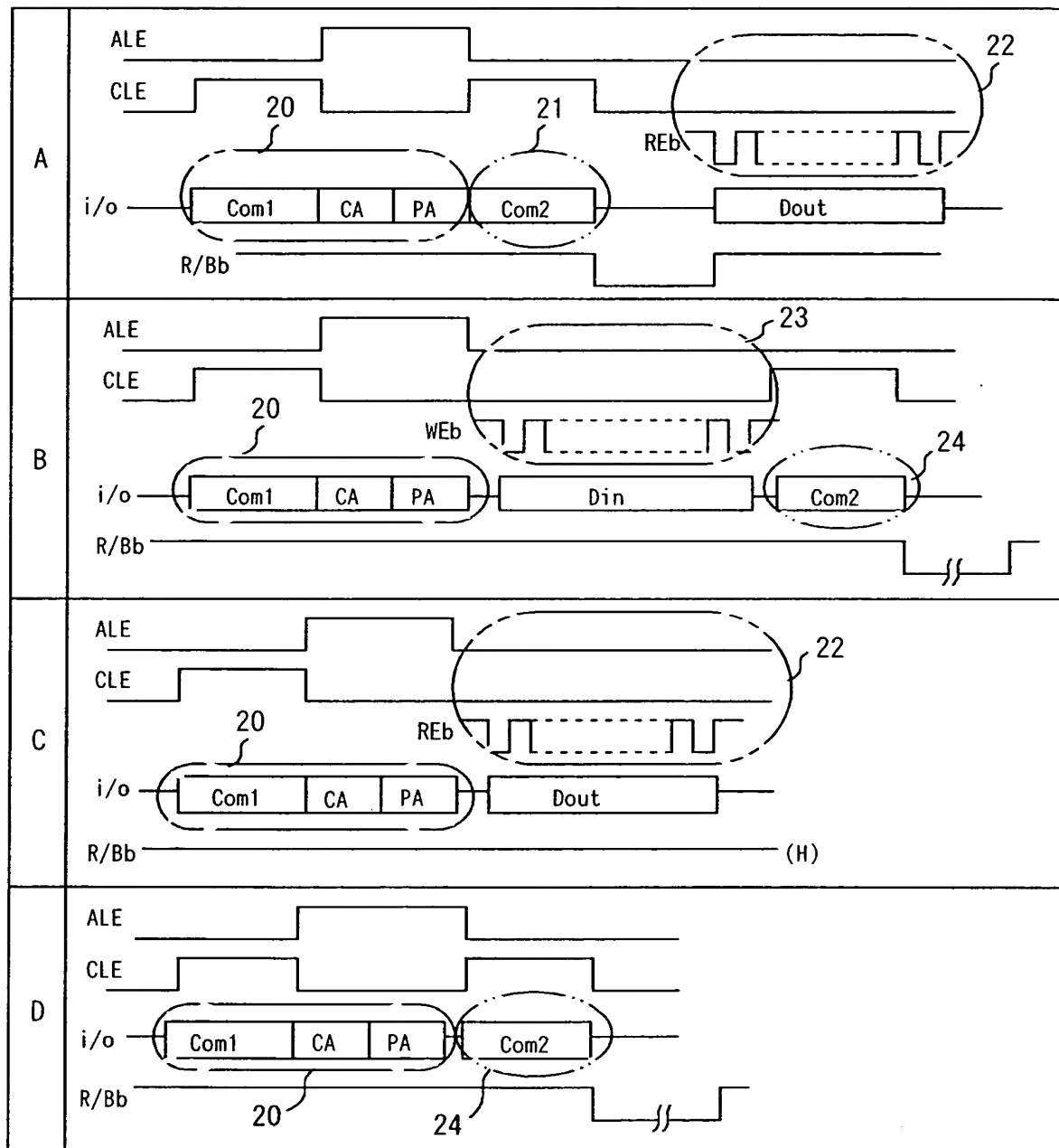


FIG.7

No.	Com1	CA	PA	Com2	BMPY CLEAR	TYPE	SUMMARY
1	00H	○	○	30H	×	Continuous 4-page (old sector) read	Read 4 continuous pages (4 pages at maximum)
2	05H	○	×	E0H	×	Set CA for Random Output in a page	Set CA in read (the optional number of times can be input)
3	06H	○	○	E1H	×	Set CA and PA for Random Output	Set CA and PA in read (the optional number of times can be input)
4	80H	○	○	11H	○	Write set-up	Set up a write
5	80H	○	○	10H	○	Write	Write for a bank set with 4 and 5 (simple upper end)
6	85H	○	×	×	×	Set CA for Random Input	Write 4 continuous pages
7	00H	○	○	35H	×	Read for a copy pack	Read 1 page for 1 bank
8	85H	○	○	10H	×	Write for a copy pack	Write data read to BMRV
9	80H	○	○	15H	○	Cache program	Open BMRV which is identical to No.5 and is not used in a write
10	60H	×	○	D0H	×	Block erase	Erase 1 block for 1 bank
11	7*H	×	×	×	×	Status read	Read a status code (70H to 76H)
12	90H	×	×	×	×	ID read	Read an ID code
13	FFH	×	×	×	×	Forcible reset	Reset an internal state and clear a status register
14	00H	○	○	31H	×	Different bank read	Read to
15	80H	○	○	12H	○	Different bank write	Write to (simple upper end)
16	80H	○	○	13H	○	Continuous 4-page write	Write data for 4 continuous pages
17	80H	○	○	16H	○	Write 2	Write having No. 5 preverify
18	80H	○	○	17H	○	Different bank write 2	Write having No. 15 preverify
19	80H	○	○	18H	○	Continuous 4-page write 2	Write having No. 16 preverify
20	00H	○	○	3AH	×	Binary read	Read in a binary mode
21	60H	○	×	D1H	×	Continuous 4-block erase	Erase 4 continuous blocks
22	FEH	×	×	×	○	Buffer clear	Clear all BMRV buffers

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FIG.8

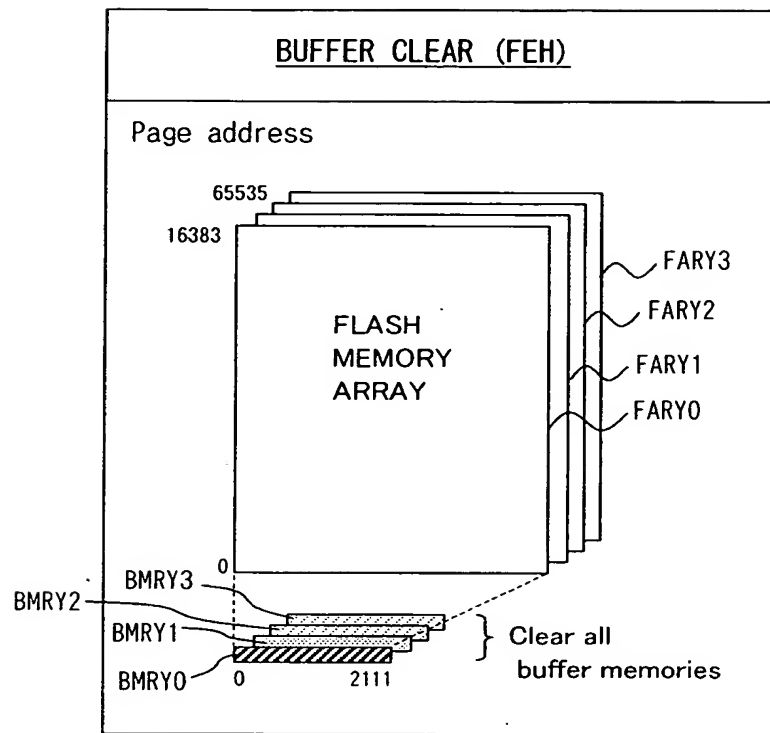


FIG.9

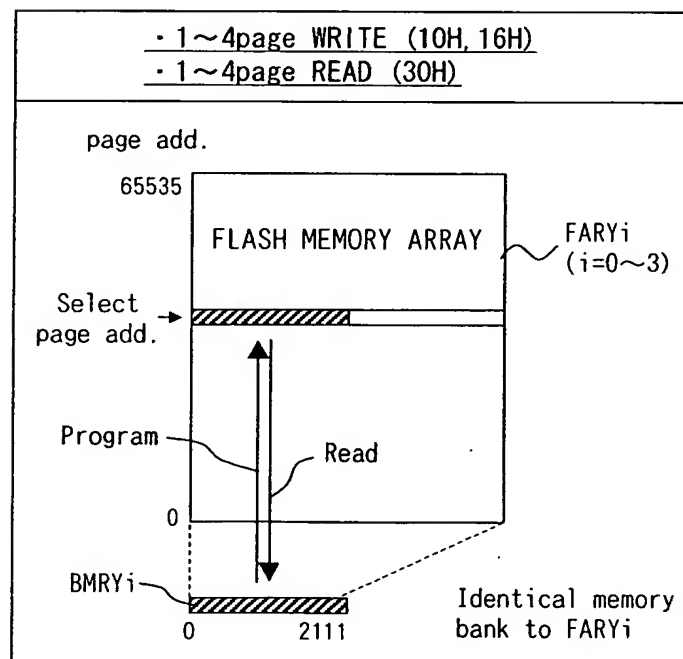


FIG.10

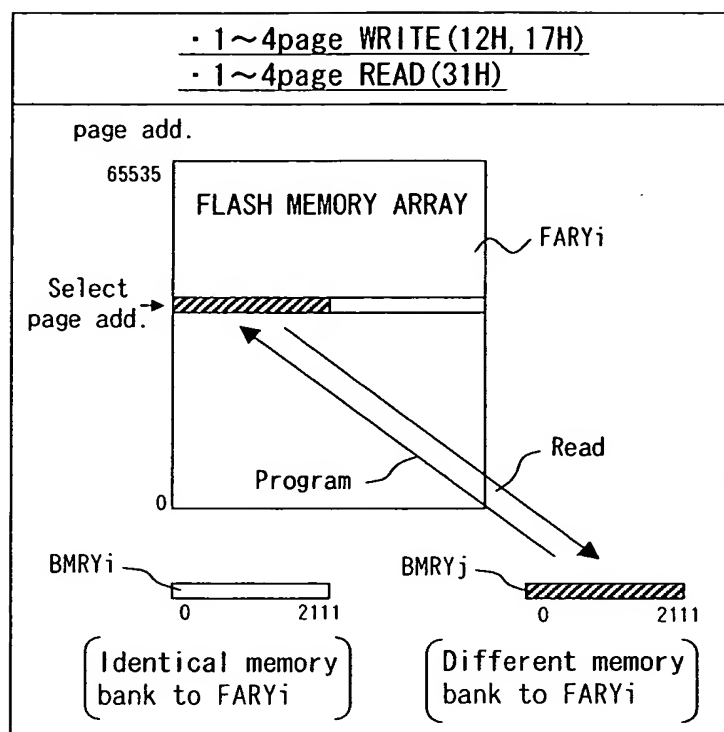


FIG.11

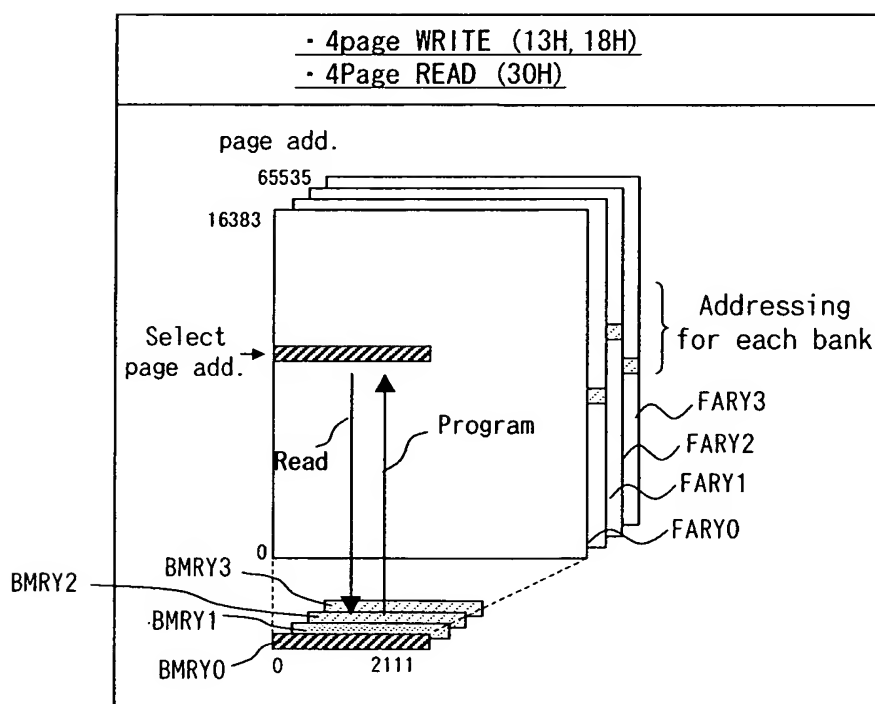


FIG.12

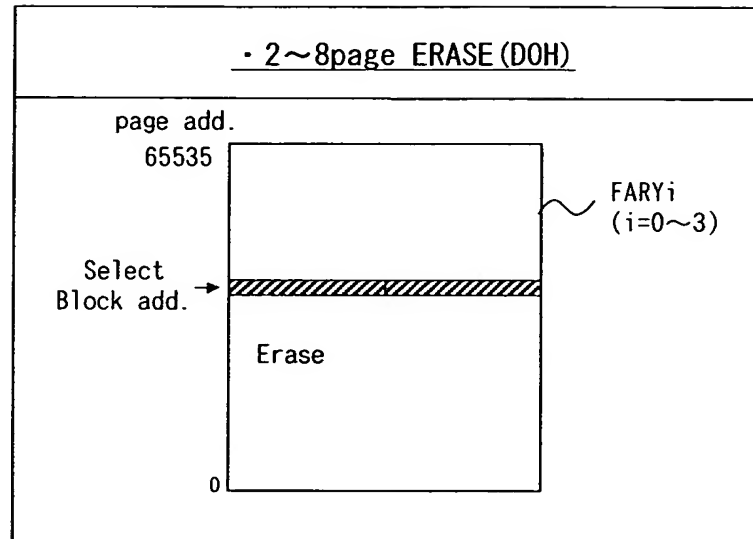


FIG.13

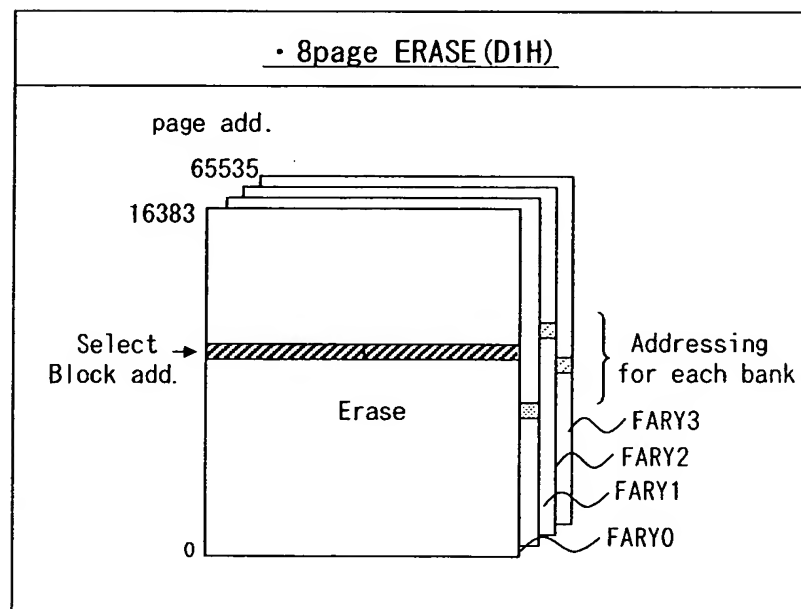


FIG.14

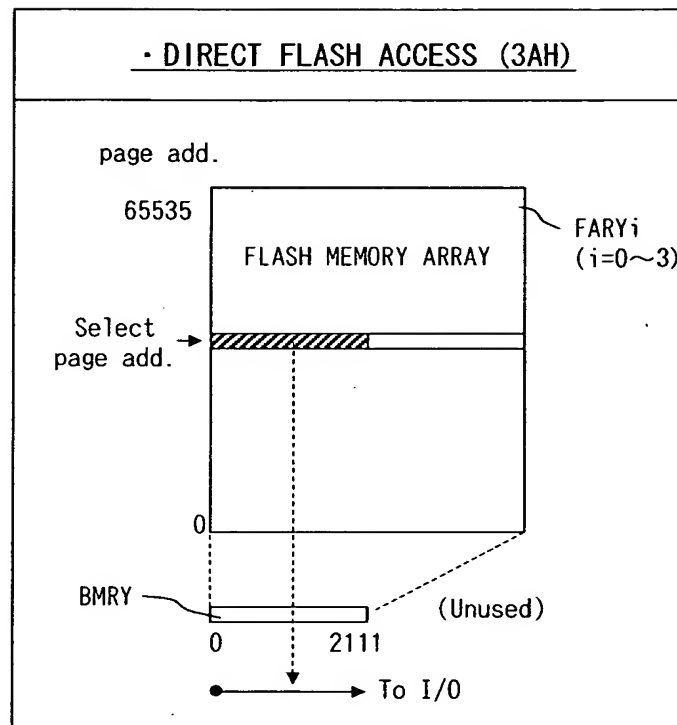


FIG.15

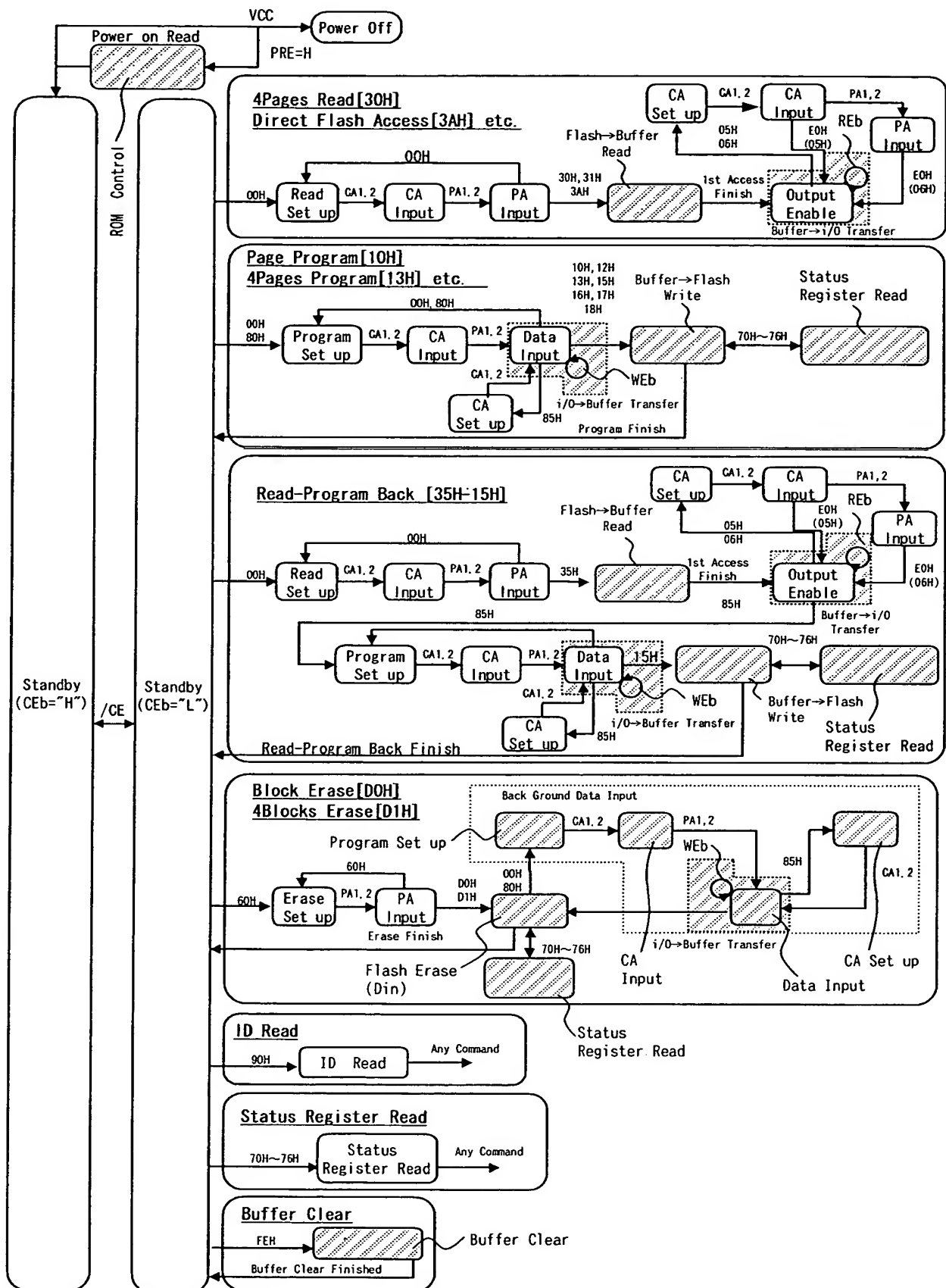


FIG.16

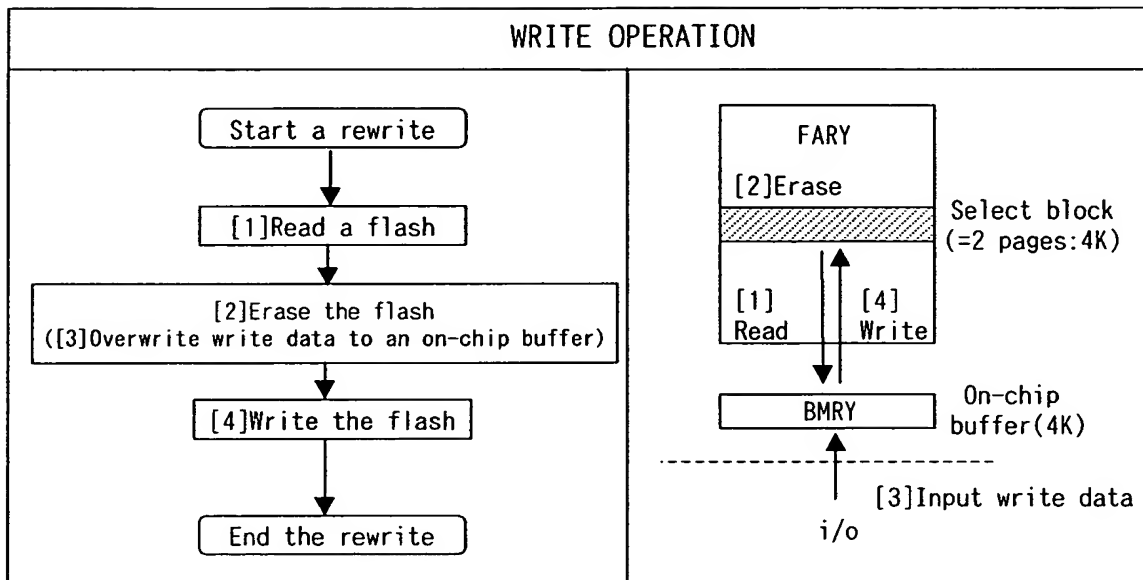


FIG.17

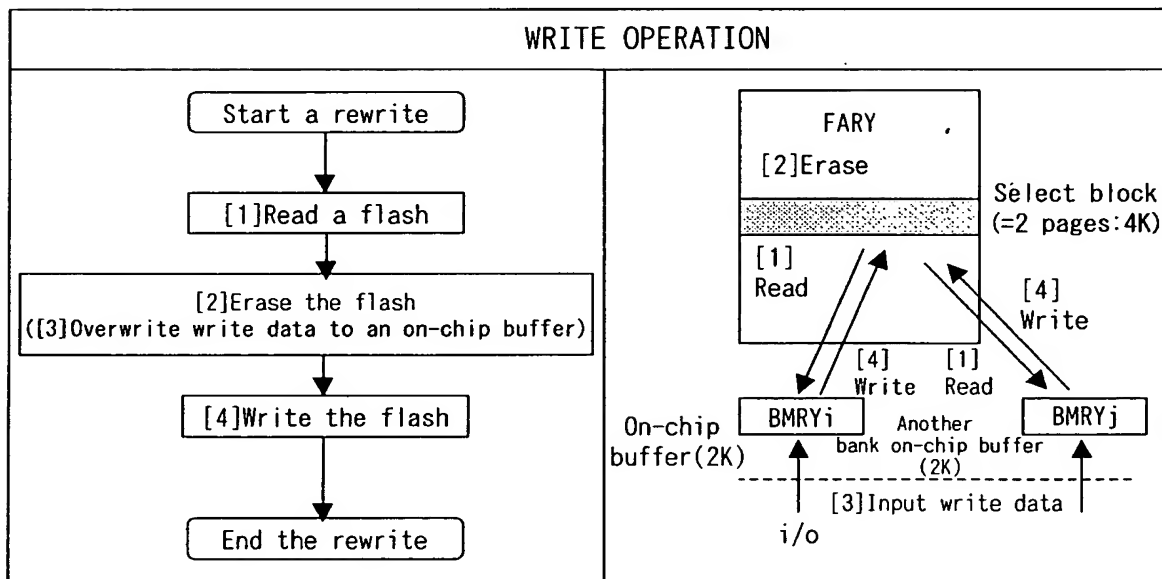


FIG.18

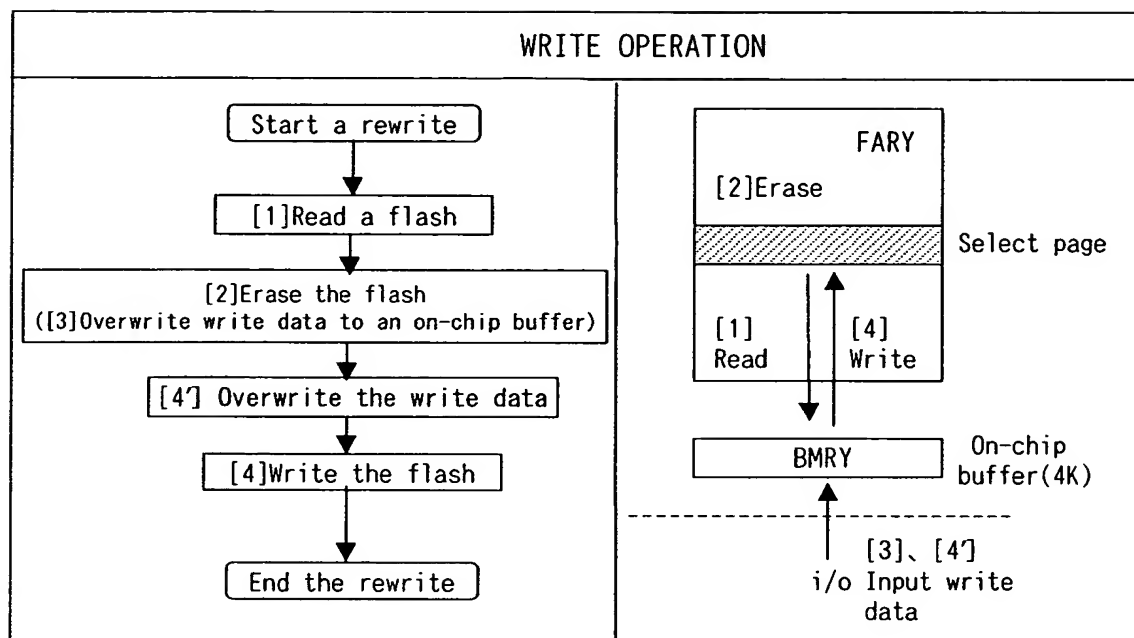


FIG.19

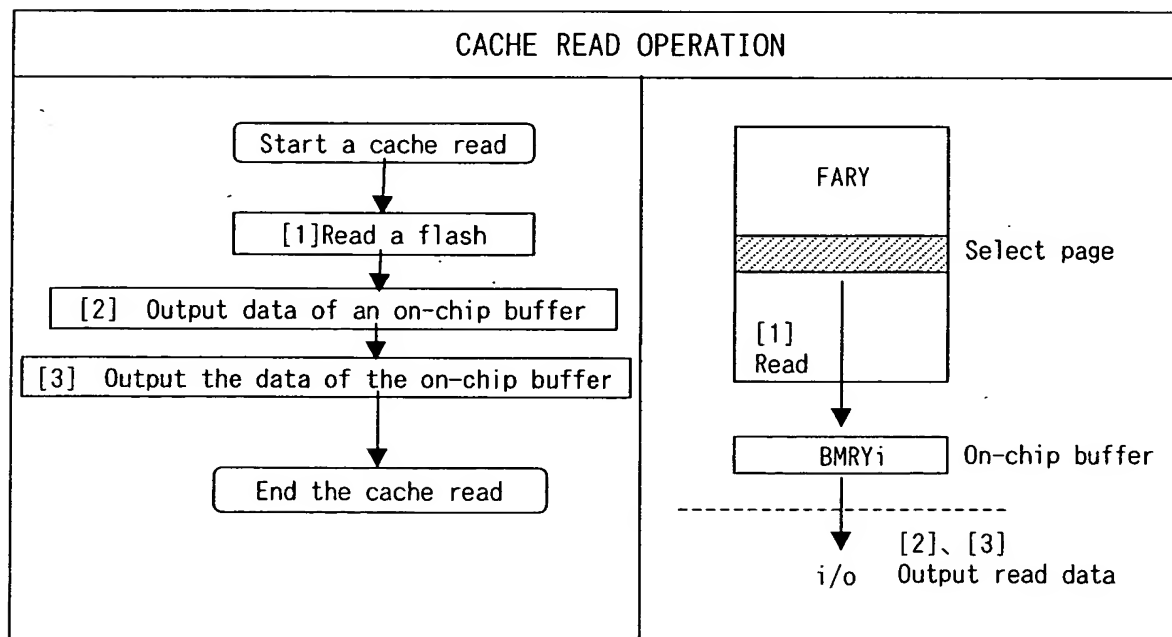


FIG.20

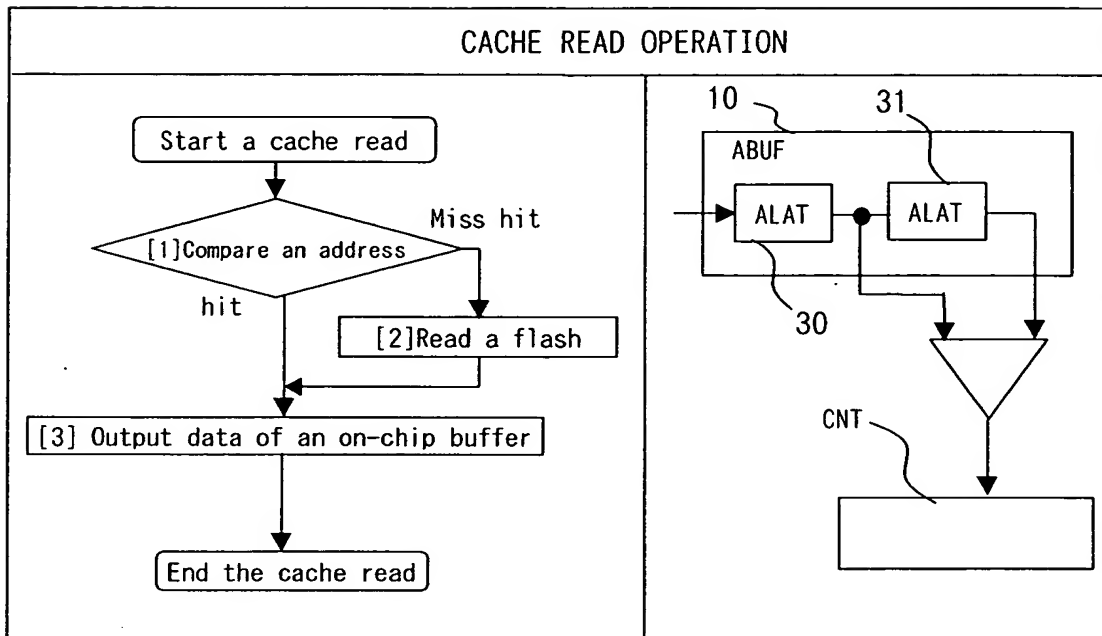


FIG.21

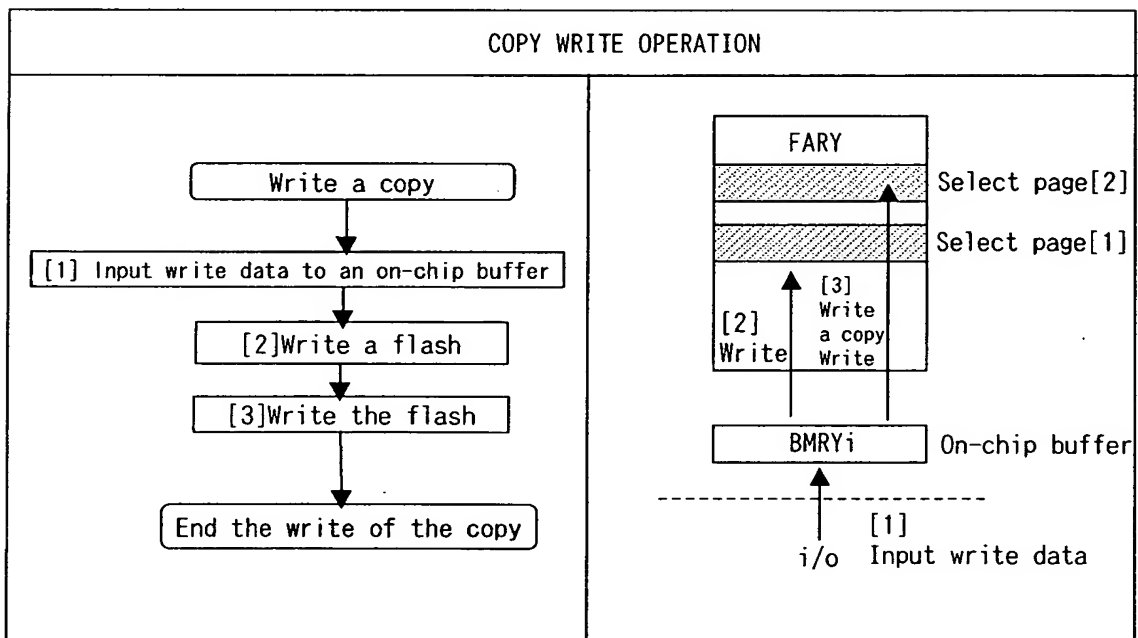


FIG.22

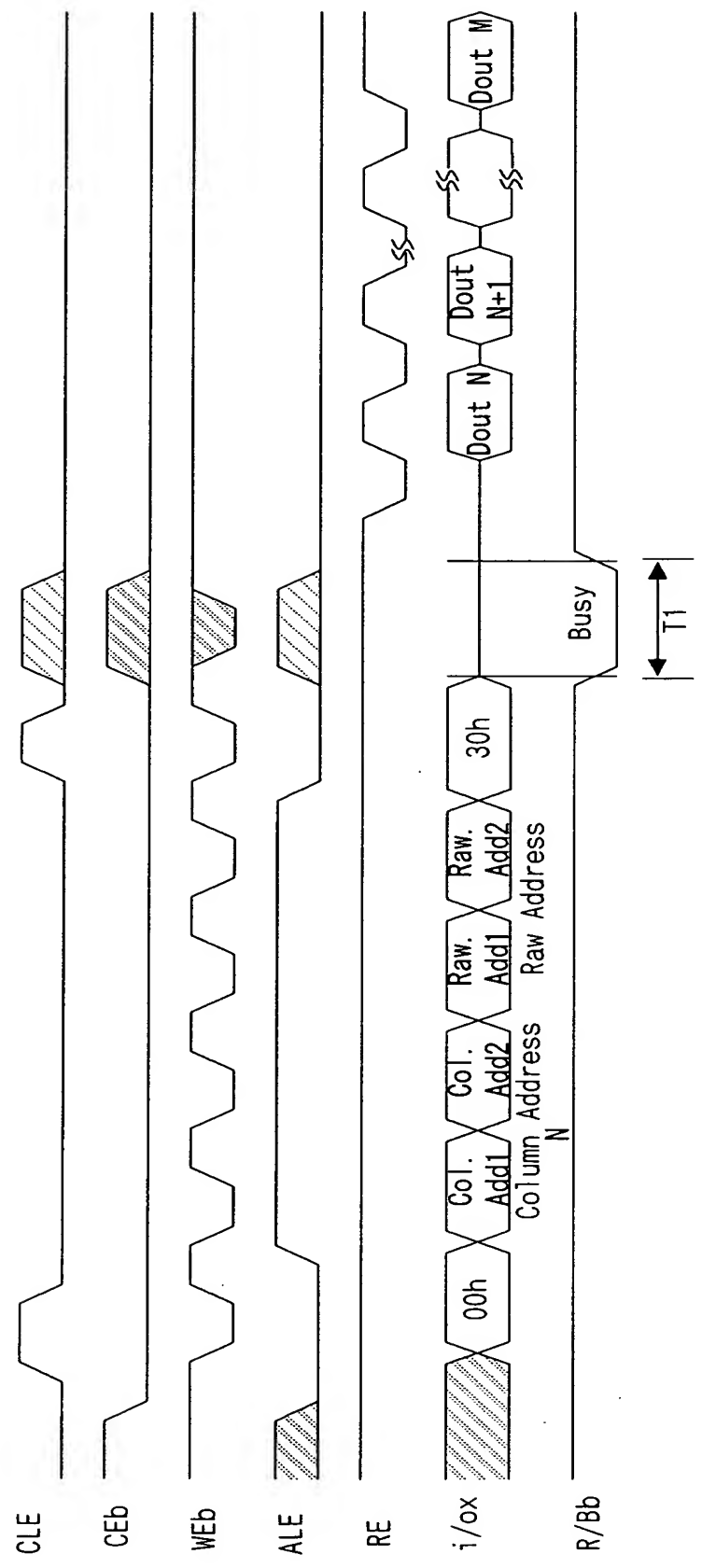


FIG.23

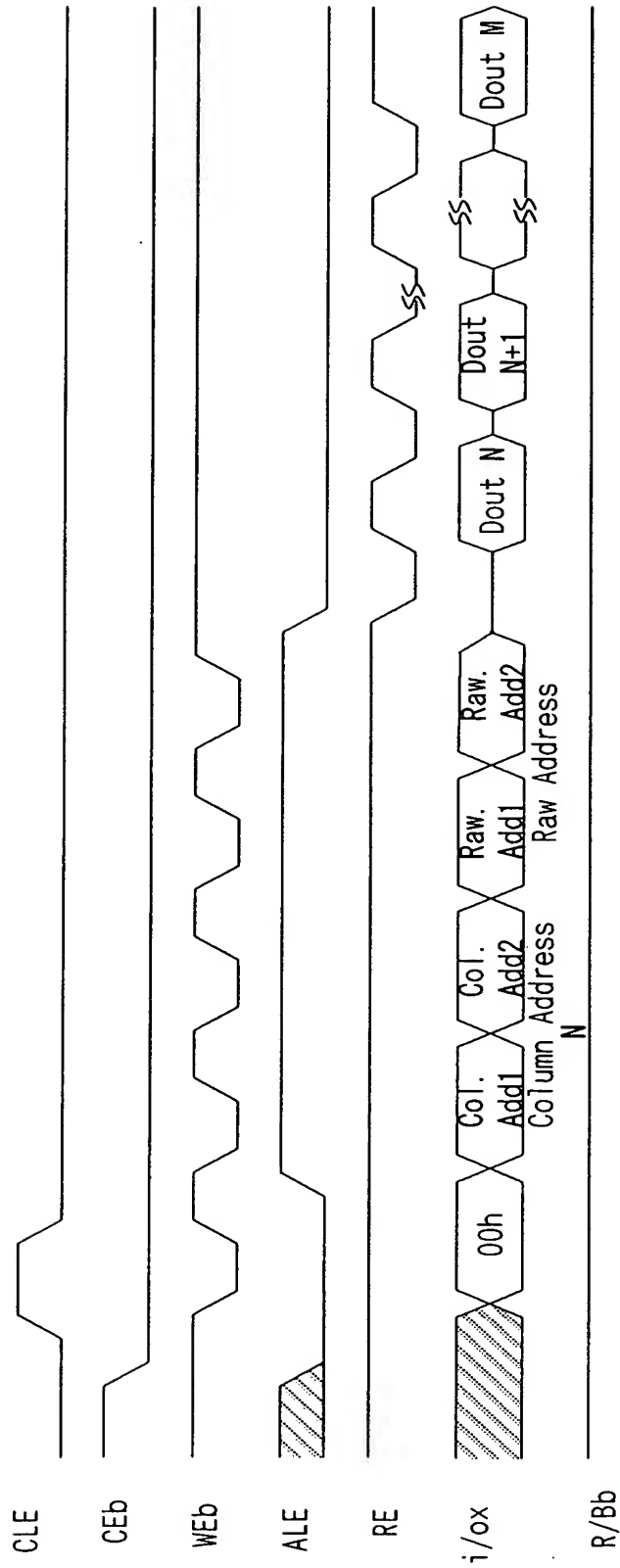
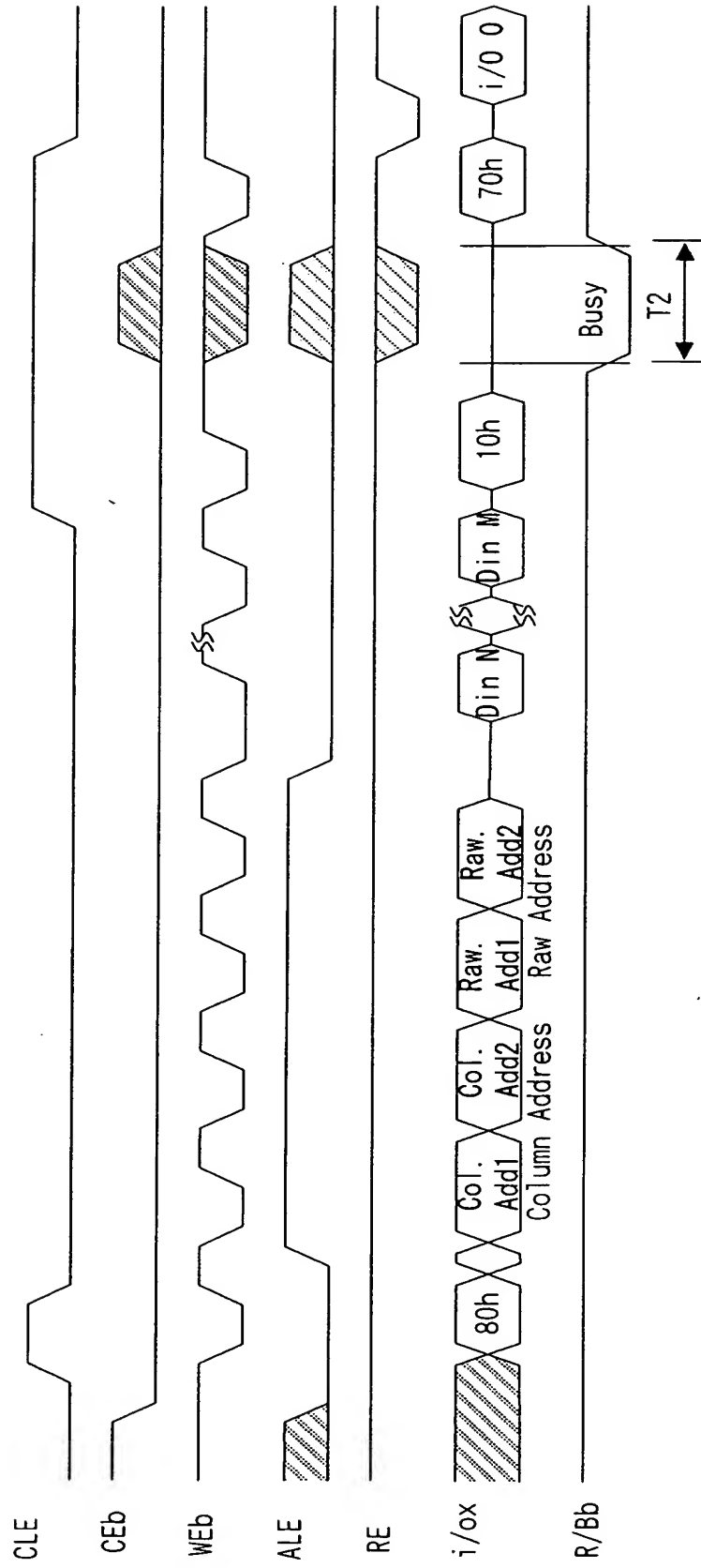


FIG.24



Timing diagram for the 74VHC163 4-bit counter. The diagram shows the waveforms for CLE, CEb, WEb, ALE, RE, i/ox, and R/Bb. CLE is a single high pulse. CEb, WEb, and ALE are periodic square waves. RE is a single high pulse. i/ox is a bus signal showing the sequence of addresses: 80h (shaded), Col. Add1, Col. Add2, Row. Add1, Row. Add2, 10h, 70h, and i/o 0. R/Bb is a signal that goes high during the 10h and 70h addresses, labeled as 'Busy'.

FIG.26

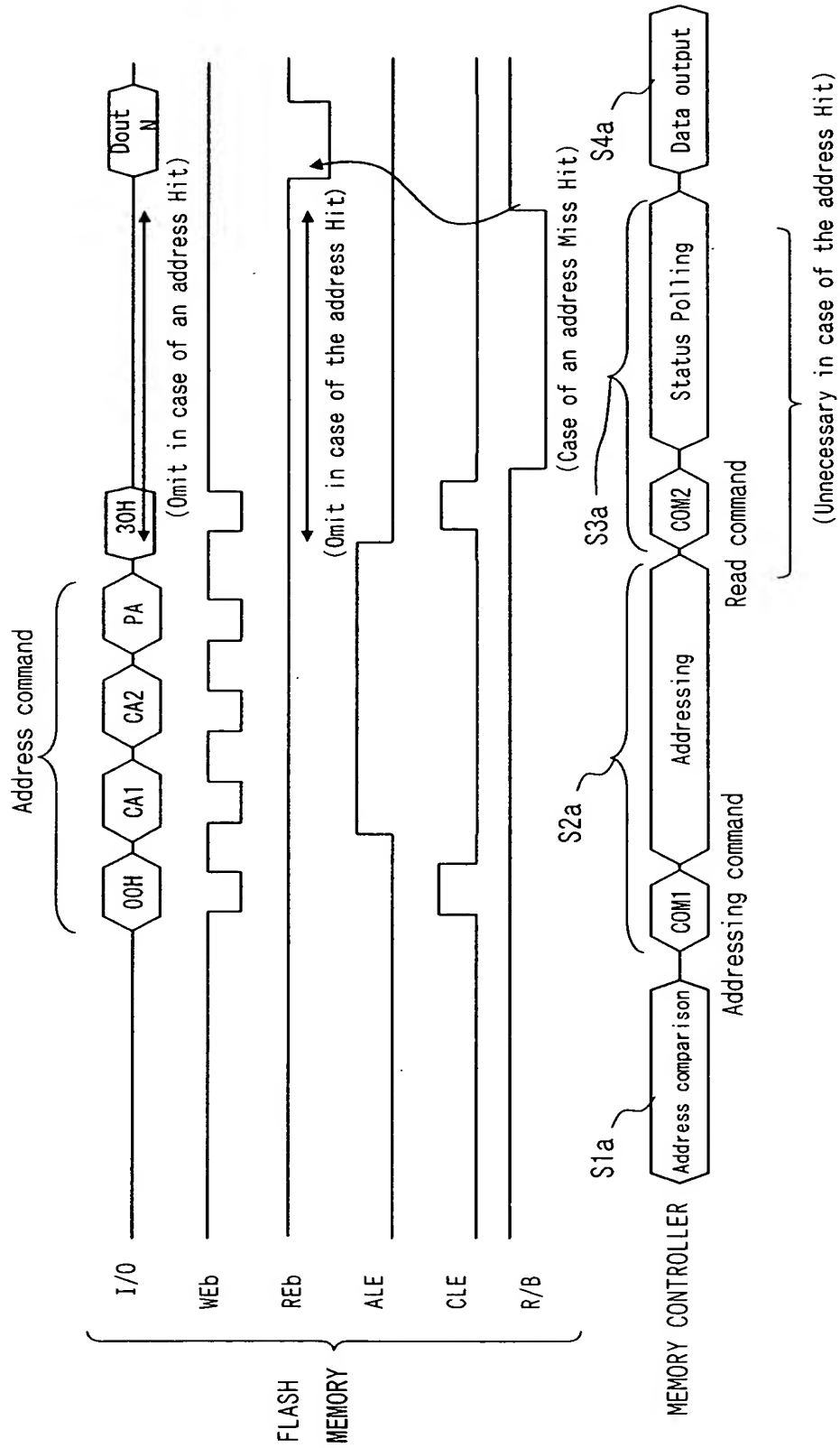


FIG. 27

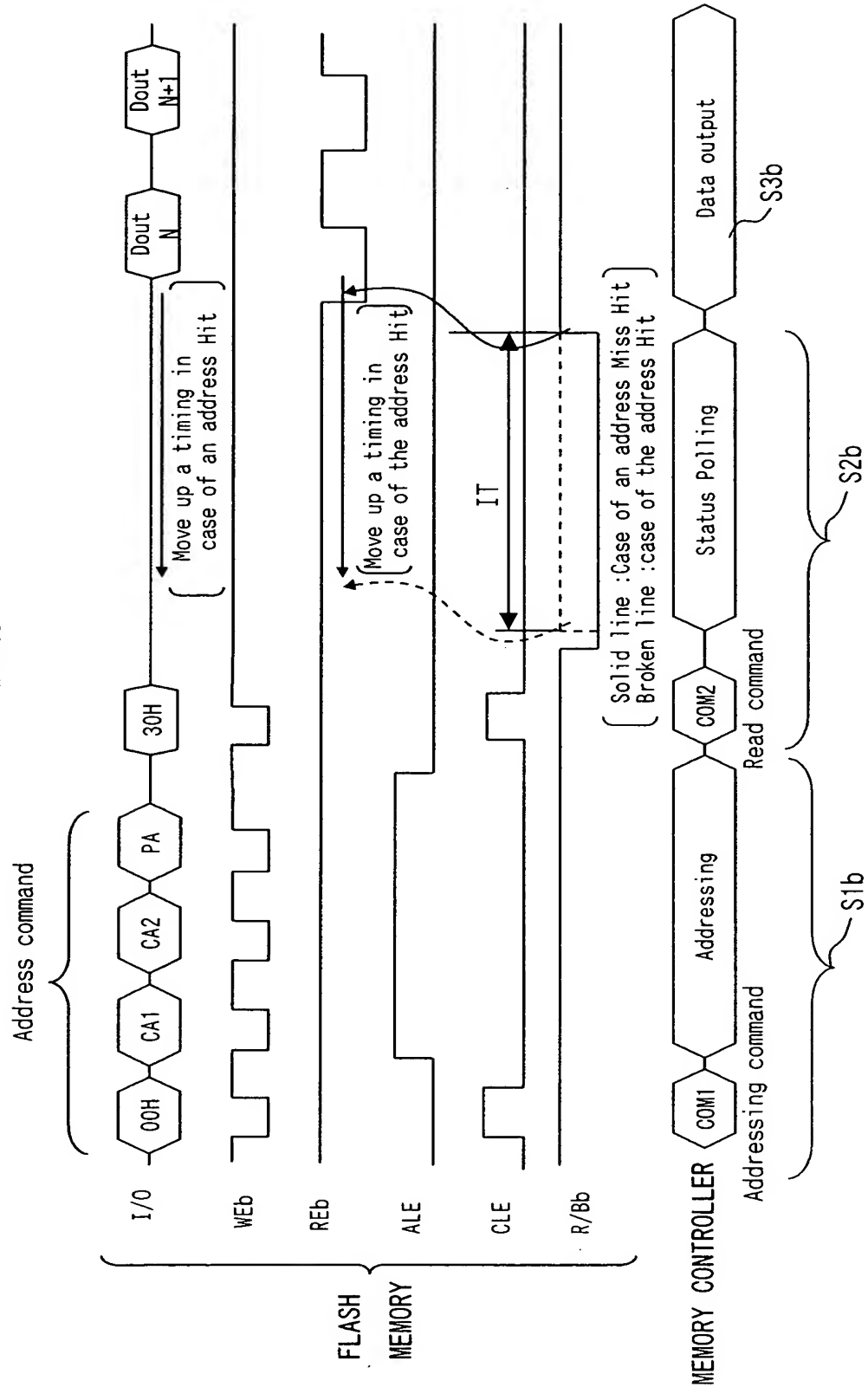


FIG.28

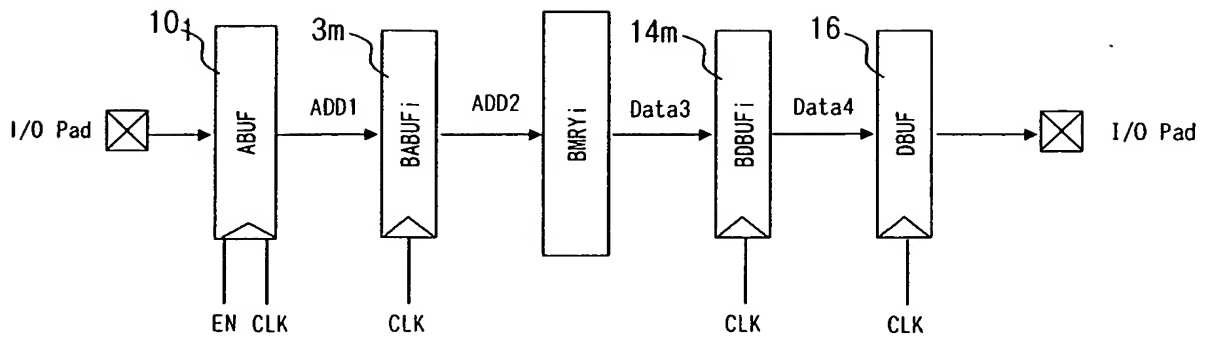


FIG.29

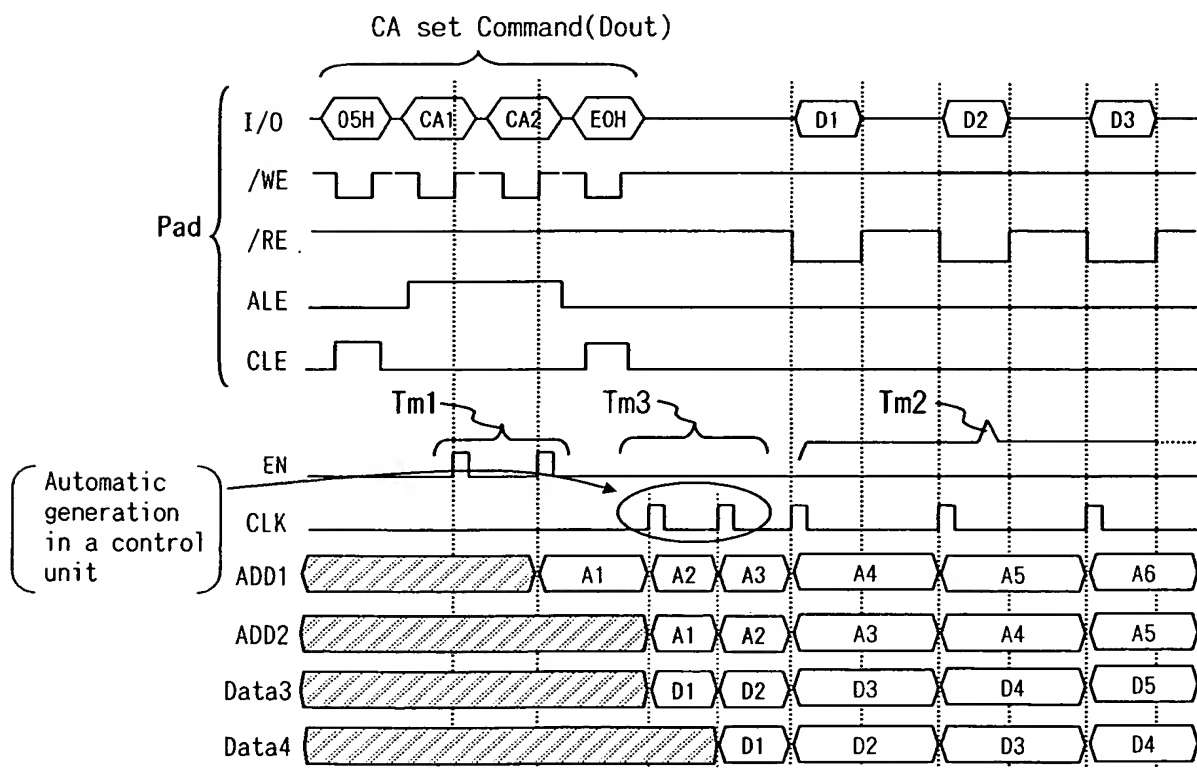


FIG.30

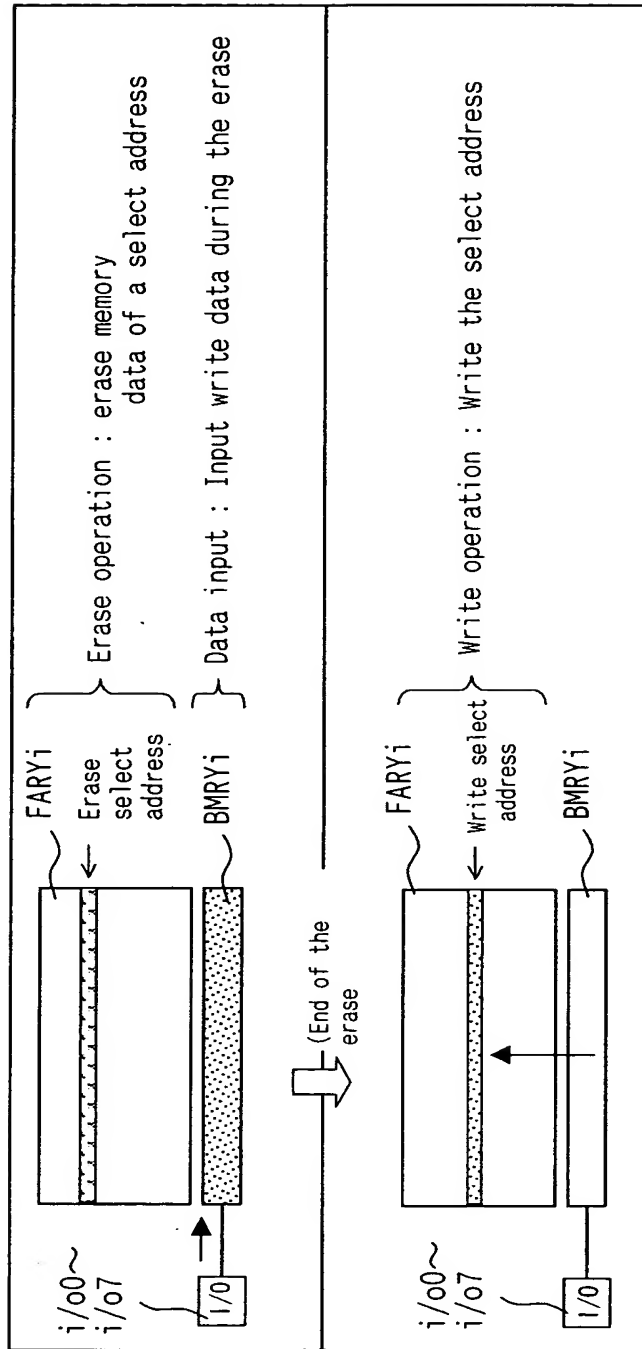


FIG.31

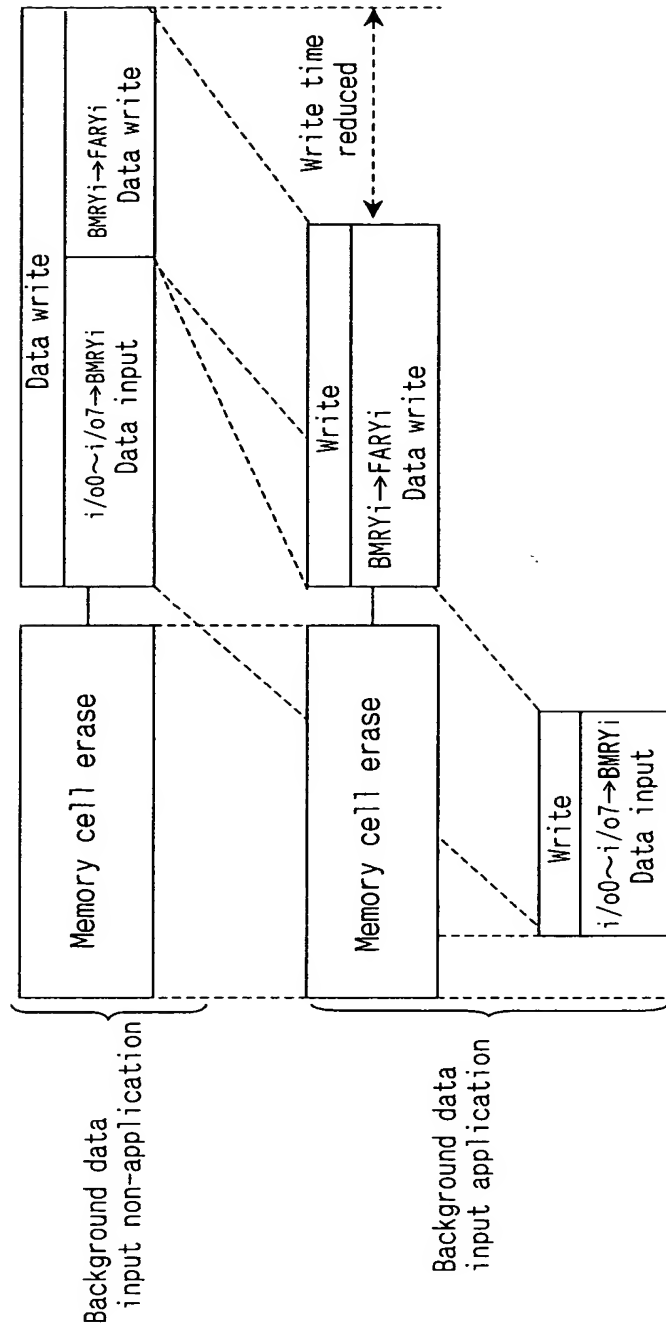


FIG. 32

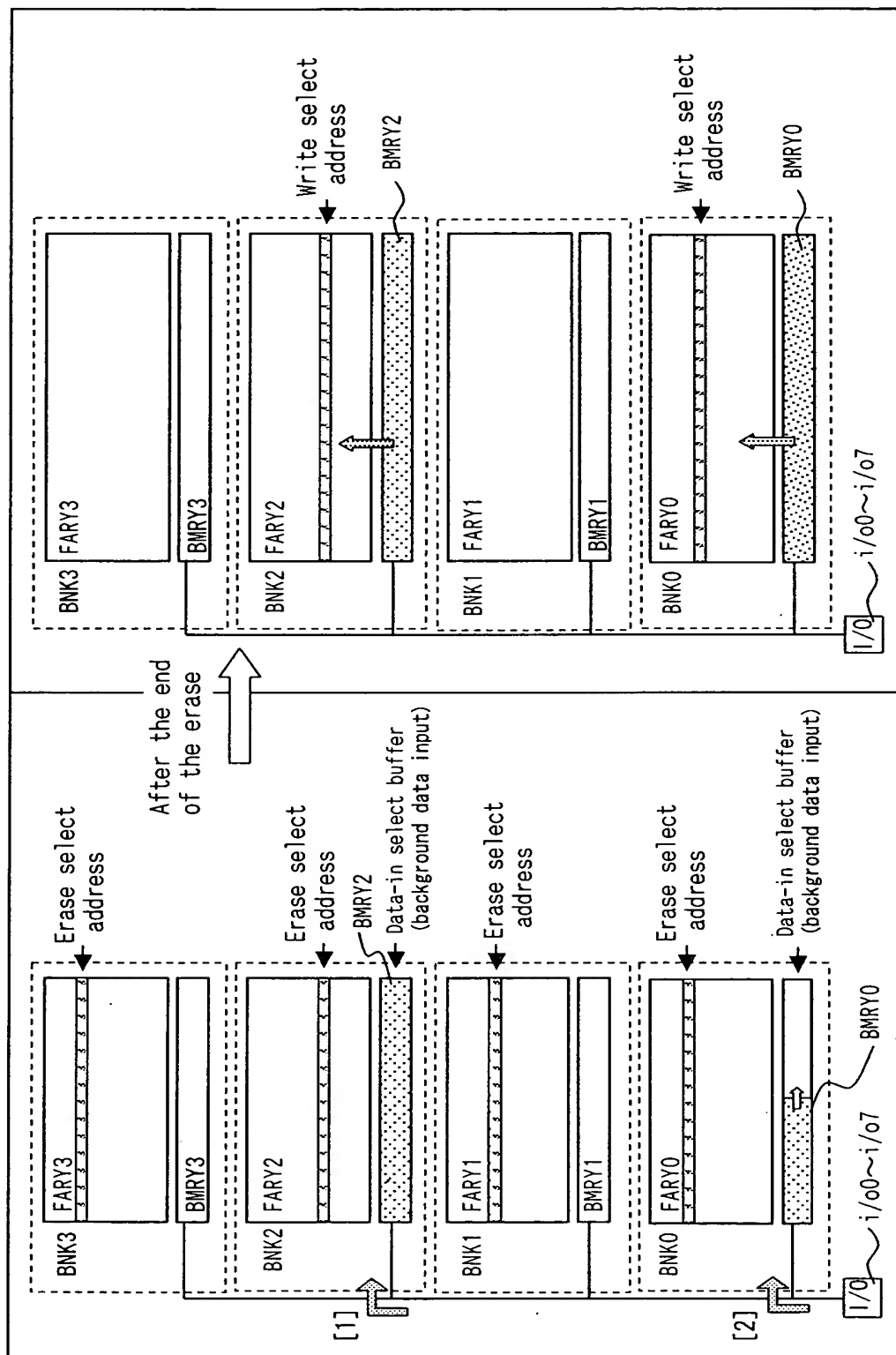


FIG.33

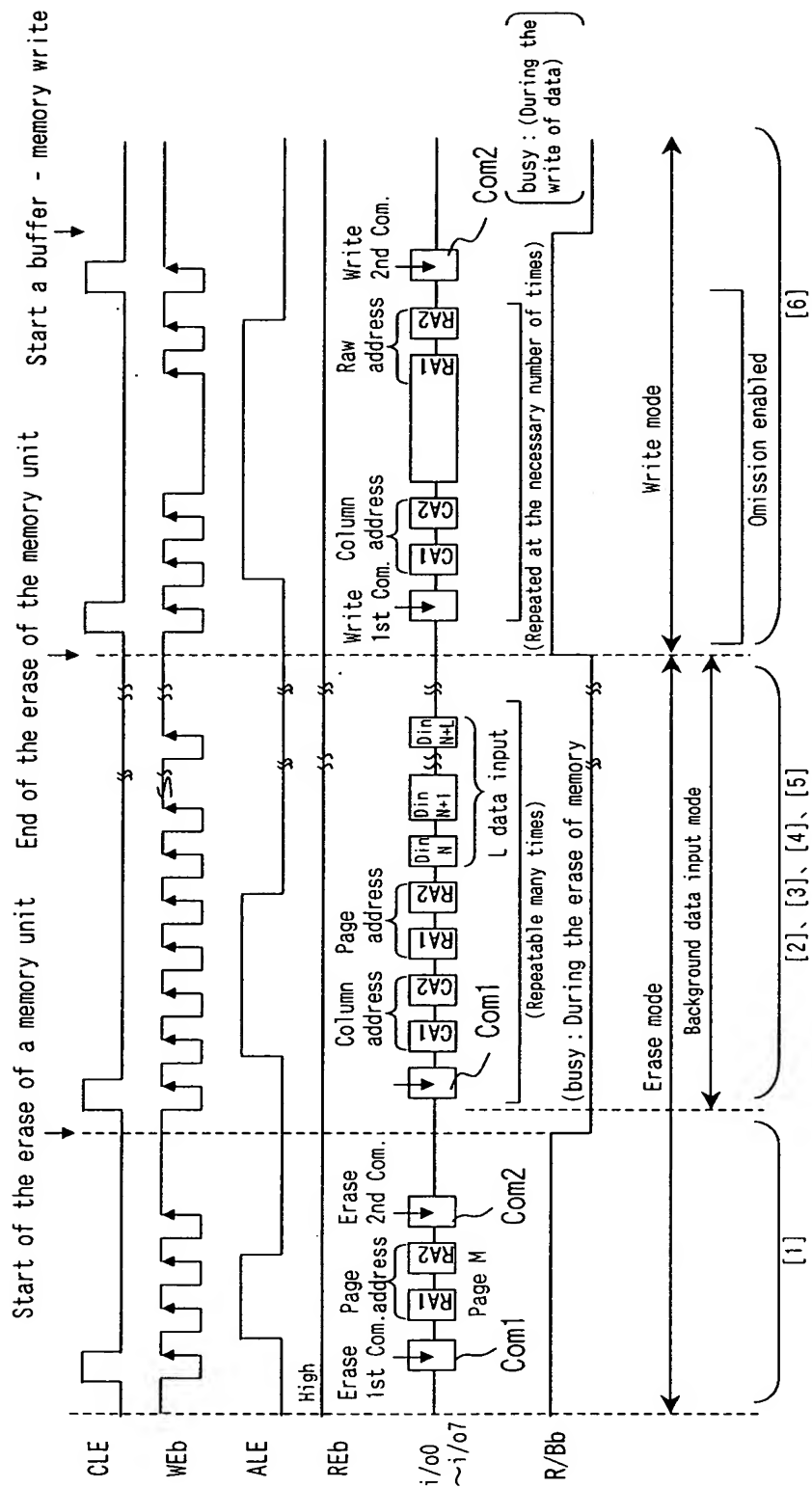


FIG.34

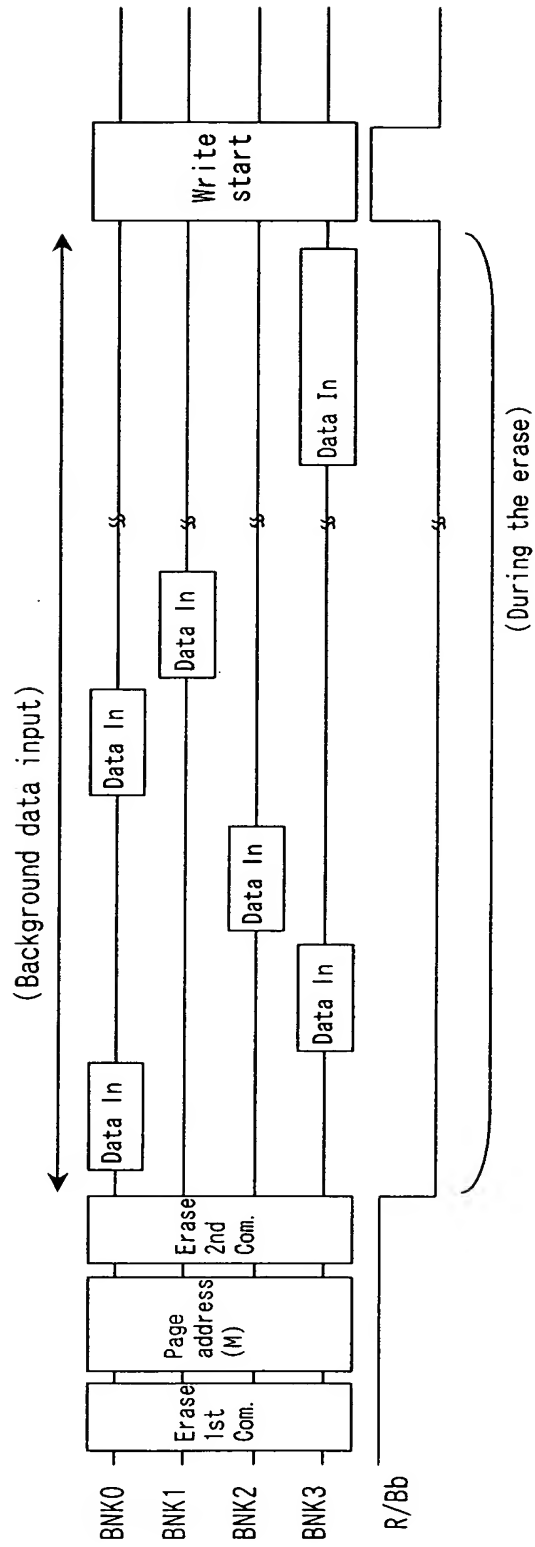
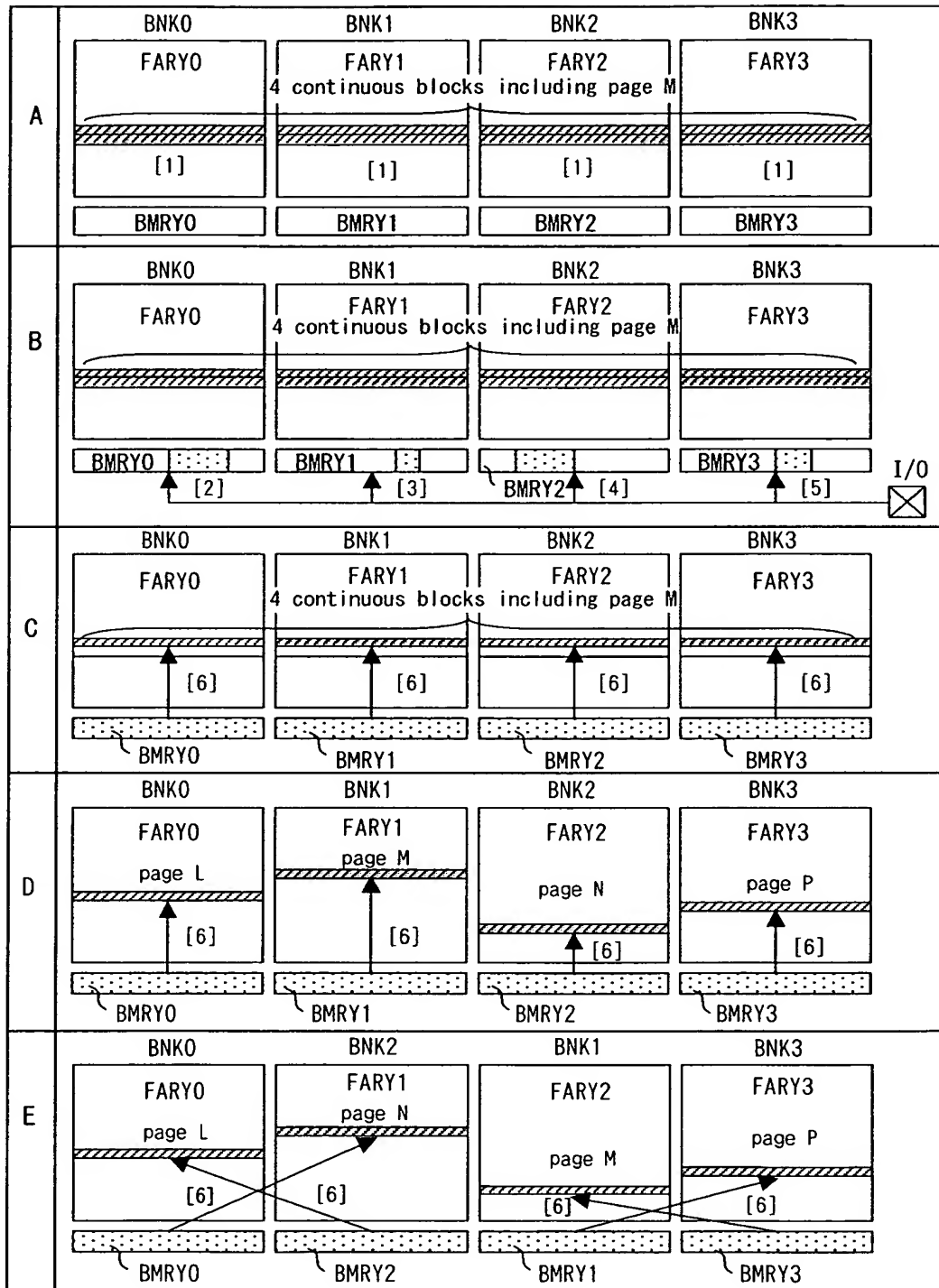


FIG.35



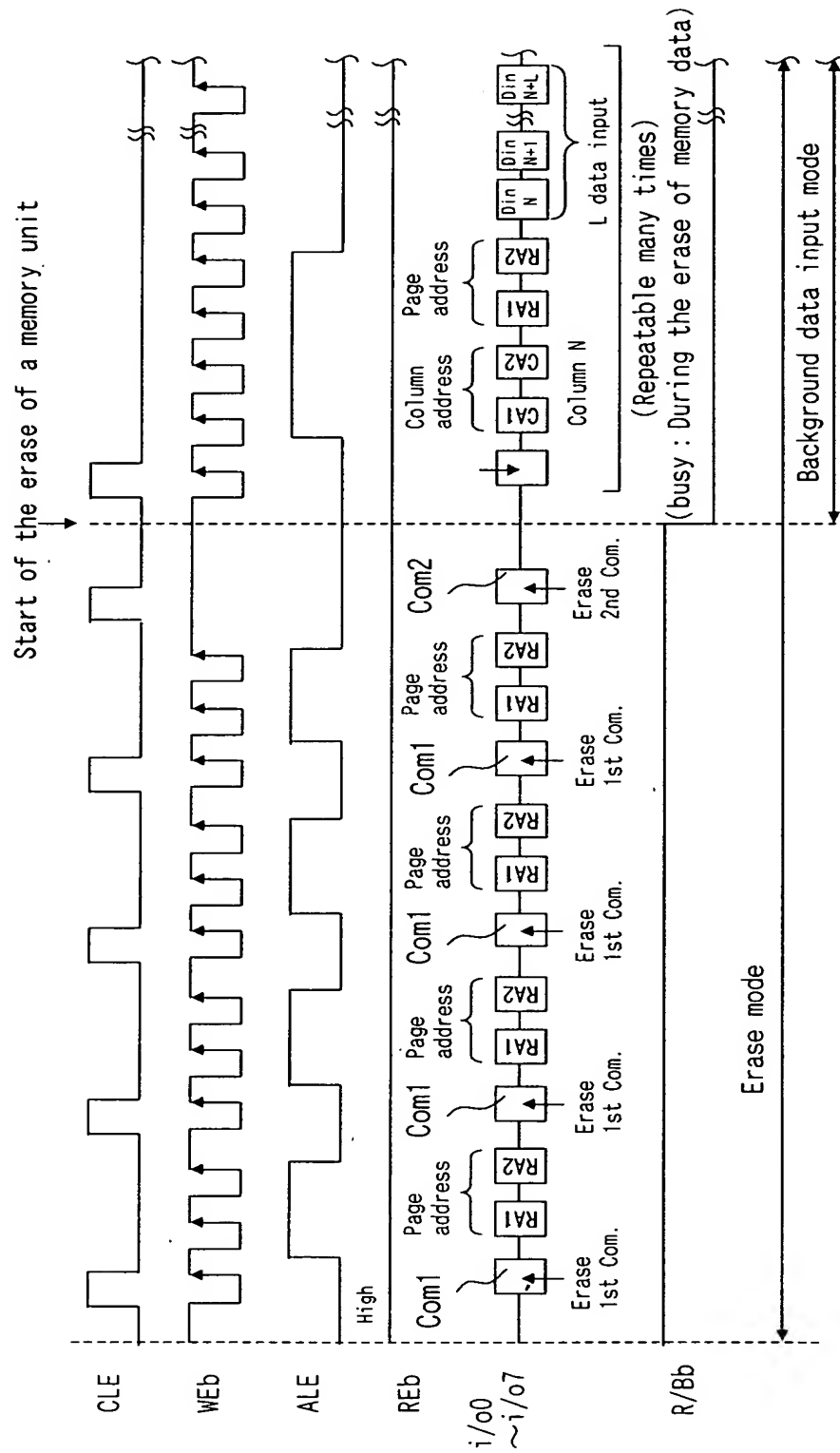


FIG.38

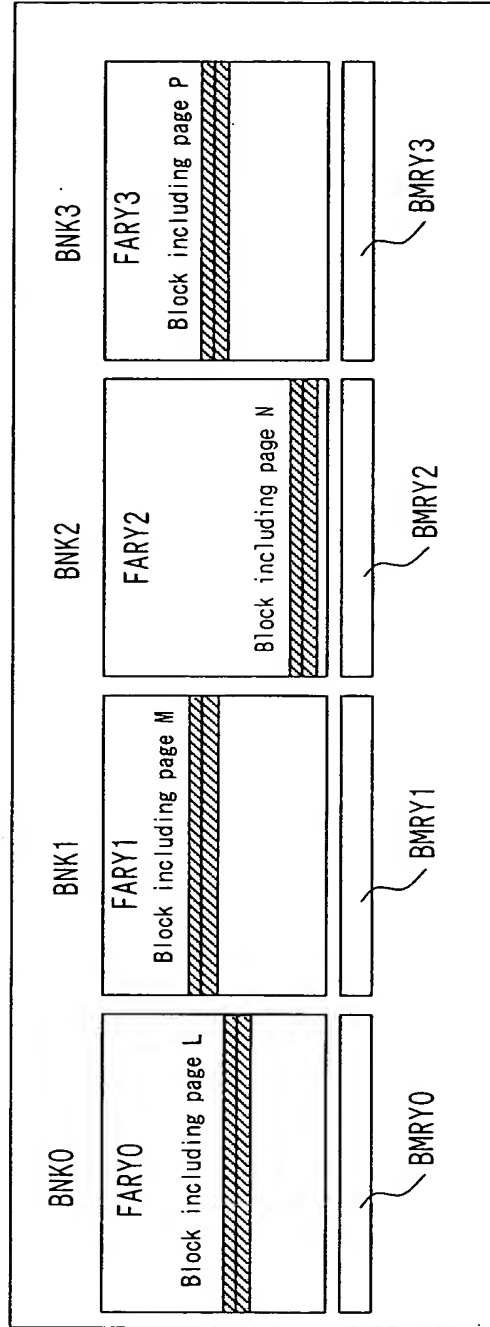


FIG.39

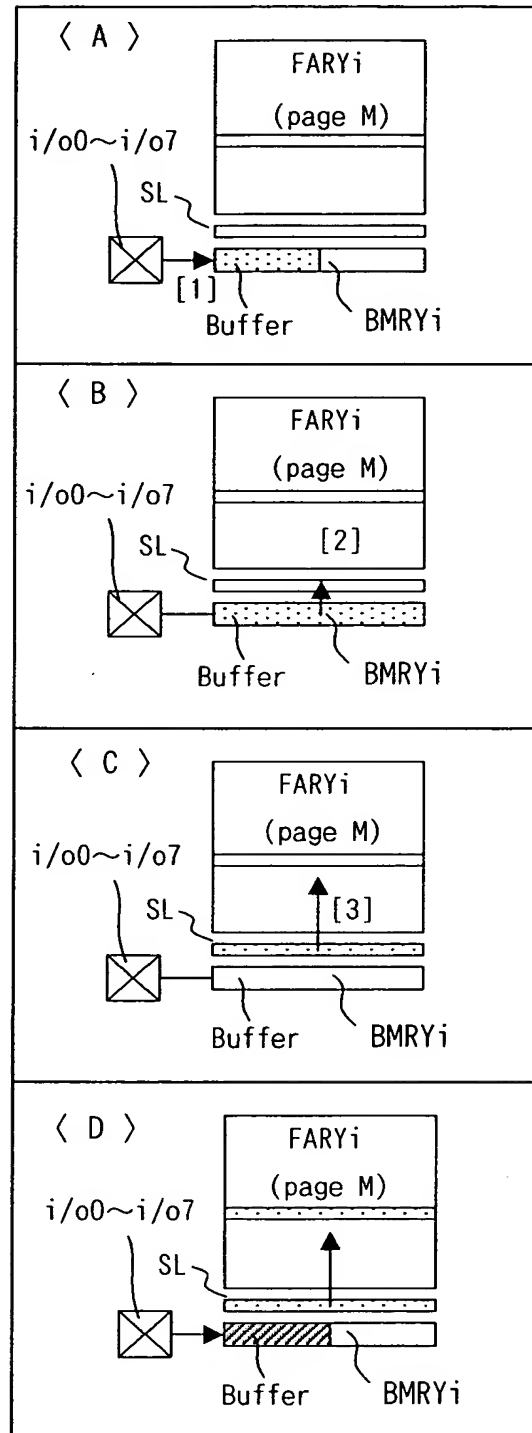


FIG. 40

